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41CL B20955 status (04/24/2012)

ITEM 1. A problem writing to the program memory space has been reported by a 41CL Beta user (Juergen Keller). Applies to initial FPGA version only. Corrected in the 07/15/2011 FPGA version.

I have set up and run a simulation of the design to investigate the problem, and can verify that the NEWT microprocessor does not always execute the WMLDL instruction properly.

To review, the WMLDL instruction (which is a NOP for the original Nut CPU) performs a write to the program memory address space, using the contents of the C register to hold both the address and data for this write. The 10-bit write data is held right-justified in C<2:0>, while the program address for this write is held in C<6:3>.

If the MMU is enabled, so that the relevant program memory address is on the 41CL board, the NEWT microprocessor automatically writes to the on-board RAM. Unfortunately, because of a logic error, if the least-significant bit of C<4> is a one, this write does not occur.

The WMLDL instruction was not originally implemented in the NEWT design, and was added in early 2010 based on customer input. Simulation was performed to verify basic operation at that time. Unfortunately no simulation was performed that happened to have the least-significant bit of C<4> set to one.

Why is this particular bit special? The new WCMD instruction, that was originally added to the NEWT to supercede the WMLDL instruction, uses this bit to distinguish read and write commands, so this bit was used to control the starting state for the memory read/write state machine. When the WMLDL instruction was added, I missed the fact that this bit conditioned the state machine starting state. So if the lsb of C<4> is zero a memory write occurs, but if the lsb is one a memory read occurs. As an aside, this is exactly why I HATE late changes.

This error only affects software that uses the WMLDL instruction. The three examples that I know of are the Assembler, HEPAX and the ZENROM.

This is one of those errors that can be repaired by reprogramming the FPGA, but that requires returning it to us unless you have access to an Actel programmer. At this point I want to wait and see if there are other issues before deciding how to proceed.

ITEM 2. A problem with the YMCPY function in the 41CL Extra Functions has been reported by a 41CL Beta user (Antti Louko). Applies to 41CL Extra Functions -1A version only.

I have stepped through the code on the V41 emulator and can verify that there are two cases where this function does not work correctly.

If the destination is a physical address and the least-significant digit of the source address is 8-F then only one transfer occurs and the YMCPY function terminates. If the destination address is logical and in internal

memory and the most-significant digit of the source address is 8-F then only one transfer occurs and the YMCPY function terminates.

The YMCPY function must update the source and destination address differently depending on the type of address being used (logical or physical). The destination address update signals the roll-over condition to the rest of the code via the S digit of a register. Unfortunately this digit is not initialized to a specific value in the case where there is no roll-over, so the digit contains stale data left over from the source address formatting section of the code. If this stale data is 8-F it is interpreted as an address rollover.

To correct this error, two locations in the YMCPY routine must be patched. Refer to the "Patching Code" section of the 41CL User Manual for instructions on how to do this. The following two locations must be patched:

address 680 must be changed to 005E (from the 00B0 that it currently contains)
address 694 must be changed to 005E (from the 00B0 that it currently contains)

ITEM 3. A anomaly with the Time module operation has been reported by a 41CL Beta user (Geoff Quickfall). Applies to all 41CL versions.

I have been able to reproduce this anomaly in my 41CL.

If the ON button on the calculator is pressed repeatedly, faster than the calculator normally turns on and off, the Time module seems to be reset.

I don't really have a way to find the root cause of this issue, but according to the timer chip datasheet there is a low-voltage detect circuit in the timer chip that resets the device. It may be possible that the power-up and power-down cycling of the FPGA is causing transients on the power line to the timer chip that are causing it to reset, but that is just an educated guess on my part.

It is very unlikely that any FPGA change or software change can modify this behavior. Because I have no intention of revising the PC board for the 41CL, we'll probably just have to live with this anomaly.

ITEM 4. A error in the 41CL User Manual has been reported by a 41CL Beta user (Matthias Wehrli). Applies to all 41CL Beta versions.

The 41CL User Manual says that a soft reset (Backspace-ON) can recover from accidentally deleting the 41CL Extra Functions (page 12 of the manual). This is not the case. Only removing power can restore the 41CL Extra Functions. The power does not need to be removed long enough to clear the memory or reset the Time module, only the few milliseconds necessary to trigger the power-on-reset function on the 41CL circuit board. The power-on-reset on the board disables the MMU, restoring access to the 41CL Extra Functions.

ITEM 5. A problem with the YIMP function in the 41CL Extra Functions has been reported by a 41CL Beta user (Antti Louko). Applies to 41CL Extra Functions -1A version only.

Using the reported symptoms I was able to identify the source of the problems in the code.

The software loops waiting for a byte to be received. Once the character available flag is recognized the software checks the status of the overrun flag to make sure that the transfer was okay. I was checking the wrong polarity for this flag, which led to the software exiting after the first byte transfer. The overflow condition was not signaled to the user because of the way that the user status is created. The incorrect polarity is tested for each byte of a word transfer, requiring two locations to be patched.

The second problem was uncovered after these first patches were applied. The section of code that updates the count for the transfer was using stale data, that was actually the last word received. If the last word was 0x0000 the test thought that the transfer was complete and exited. This required one more location to be patched.

To correct these errors, three locations in the YIMP routine must be patched. Refer to the "Patching Code" section of the 41CL User Manual for instructions on how to do this. The following three locations must be patched:

address F51 must be changed to 03B3 (from the 03BB that it currently contains)
address F6A must be changed to 0343 (from the 0347 that it currently contains)
address F7A must be changed to 02C3 (from the 02C7 that it currently contains)

ITEM 6. A problem with the YFWR function in the 41CL Extra Functions has been reported by a 41CL Beta user (Antti Louko). Applies to 41CL Extra Functions -1A version only.

Using the reported symptoms (no flash write, even though the function required the normal amount of time to complete) I was able to identify the source of the problem in the code.

The Flash memory requires a sequence of "unlock" commands before it will perform a write. These commands are to specific addresses, with specific data, in a particular order. The software does all of the writes in the correct sequence, but the most-significant bit of the address happens to be set to one for two of the writes. The Flash doesn't care about this, but this bit routes the writes to the RAM chip select instead of to the Flash chip select. Further proof that I am not a programmer.

To correct these errors, eight locations in the YFWR routine must be patched. Refer to the "Patching Code" section of the 41CL User Manual for instructions on how to do this. The following eight locations must be patched:

address DFD must be changed to 0010 (from the 0090 that it currently contains)
address DFE must be changed to 0110 (from the 0290 that it currently contains)
address DFF must be changed to 0010 (from the 0290 that it currently contains)
address E00 must be changed to 0150 (from the 025C that it currently contains)
address E01 must be changed to 0150 (from the 0110 that it currently contains)
address E08 must be changed to 02AA (from the 00AA that it currently contains)
address E31 must be changed to 013C (from the 00BC that it currently contains)
address E4C must be changed to 013C (from the 00BC that it currently contains)

ITEM 7. A problem with the YFERASE function in the 41CL Extra Functions has been reported by a 41CL Beta user (Antti Louko). Applies to 41CL Extra Functions -1A version only.

Antti was able to develop this patch himself, based on the patch I developed for the YFWR function.

To correct these errors, ten locations in the YFERASE routine must be patched. Refer to the "Patching Code" section of the 41CL User Manual for instructions on how to do this. The following ten locations must be patched:

address D1B must be changed to 0110 (from the 0150 that it currently contains)
address D51 must be changed to 0010 (from the 0090 that it currently contains)
address D52 must be changed to 0110 (from the 0290 that it currently contains)
address D53 must be changed to 0010 (from the 0290 that it currently contains)

address D54 must be changed to 0150 (from the 025C that it currently contains)
address D55 must be changed to 0150 (from the 0110 that it currently contains)
address D5C must be changed to 02AA (from the 00AA that it currently contains)
address D7E must be changed to 013C (from the 00BC that it currently contains)
address D88 must be changed to 013C (from the 00BC that it currently contains)
address D97 must be changed to 013C (from the 00BC that it currently contains)

ITEM 8. A change in the time-out period for the serial functions has been requested by a Beta user (Roger Schoenthal). Applies to 41CL Extra Functions -1A version only.

Currently the timeout period is fairly short when in Turbo mode (like 475mS in 50x). This can make it hard to start a YIMP without losing data or timing out. This timeout period can be increased by a factor of four, to 1.9s.

To change the timeout limits for YPUT and YGET change the following locations:

address EAC must be changed to 0046 (from the 0130 that it currently contains)
address EAD must be changed to 02A6 (from the 03FF that it currently contains)

To change the timeout limits for YEXP and YIMP change the following locations:

address F1E must be changed to 0046 (from the 0130 that it currently contains)
address F1F must be changed to 02A6 (from the 03FF that it currently contains)
address F3B must be changed to 0046 (from the 0130 that it currently contains)
address F3C must be changed to 02A6 (from the 03FF that it currently contains)
address F6E must be changed to 0046 (from the 0130 that it currently contains)
address F6F must be changed to 02A6 (from the 03FF that it currently contains)

ITEM 9. There have been several requests for additional functions to be included in the 41CL Extra Functions. Applies to 41CL Extra Functions -1A version only.

Some of these requests are planned for a 1C revision to YFNS. All are currently being debugged. After these functions are added there is not much room left in the YFNS image.

PLUGP and UPLUGP insert and remove a 4K module from Page 6.

PLUGH and UPLUGH insert and remove a 4K module from Page 7.

YSEC is a one second delay, that is independent of the current Turbo mode.

YFNS? returns to current location (the page number, in the range 6-15) of the YFNS image in the X register.

These functions are added to end of the FAT, so they do not change existing function numbers. Current locations of all entry point are preserved. There are over 100 lines needed to implement these functions, so it may not be practical to enter them as patches. But I can supply the addresses and data if anyone wants to try it.

ITEM 10. The 41CL Extra Functions take advantage of a special feature of the NEWT microprocessor. Applies to all versions of the 41CL Extra Functions.

The NEWT microprocessor in the 41CL contains a feature that allows tagging instructions for execution at normal speed, independent of the current Turbo mode. This feature is required to maintain compatibility with the original 41C when timing loops are used, and is used multiple times in the OS for example.

The YFERASE and YSEC functions take advantage of this feature to generate the delays that those functions require. Unfortunately the .rom file format that is commonly used to distribute module images does not support this tagging of instructions. As a result, any 41CL Extra Functions image that is loaded using this file format will need to be patched to add the 1x execution tags. For YFNS-1C and later, the following locations need to be patched for YFERASE and YSEC to function properly when executed shile in a Turbo mode. These patches are not required when the functions are executed at normal speed.

address 1F3 must be changed to 326E (from the 026E that the .rom file contains)
address 1F4 must be changed to 33FB (from the 03FF that the .rom file contains)
address D92 must be changed to 326E (from the 026E that the .rom file contains)
address D93 must be changed to 33FB (from the 03FB that the .rom file contains)

This item (number 10) has been resolved and no longer applies **ONLY** if the .rom file is transferred over the serial port. If the .rom file is transferred via actual hardware (CLONIX, NOVRAM, MLDL, etc.) then the special tag bits will be lost, and the patch **MUST** be applied for proper operation in Turbo mode.

ITEM 11. The new PLUGP and PLUGH functions do not work properly with either the -RAM or the -16K identifiers. Applies to 41CL Extra Functions -1C version only.

A coding mistake allows the internal subroutine stack to overflow when either if these identifiers is used. This error is corrected in the 41CL Extra Functions -1E version. The -1D version also corrects this, but is not an official release.

ITEM 12. The time delay before a keypress is NULLed is affected by the Turbo mode. (Eric Smith). Applies to all 41CL Beta versions.

The timing loop that sets the delay before a keypress is NULLed was missed in the OS. It should have been tagged to run at 1x speed to make the delay independent of the Turbo mode.

ITEM 13. The YFWR function does not prevent writing to the OS area! NEVER try to write to the OS area of the Flash, or you will brick your calculator!

This warning applies to ALL versions of YFNZ (and YFNS) prior to -3B.