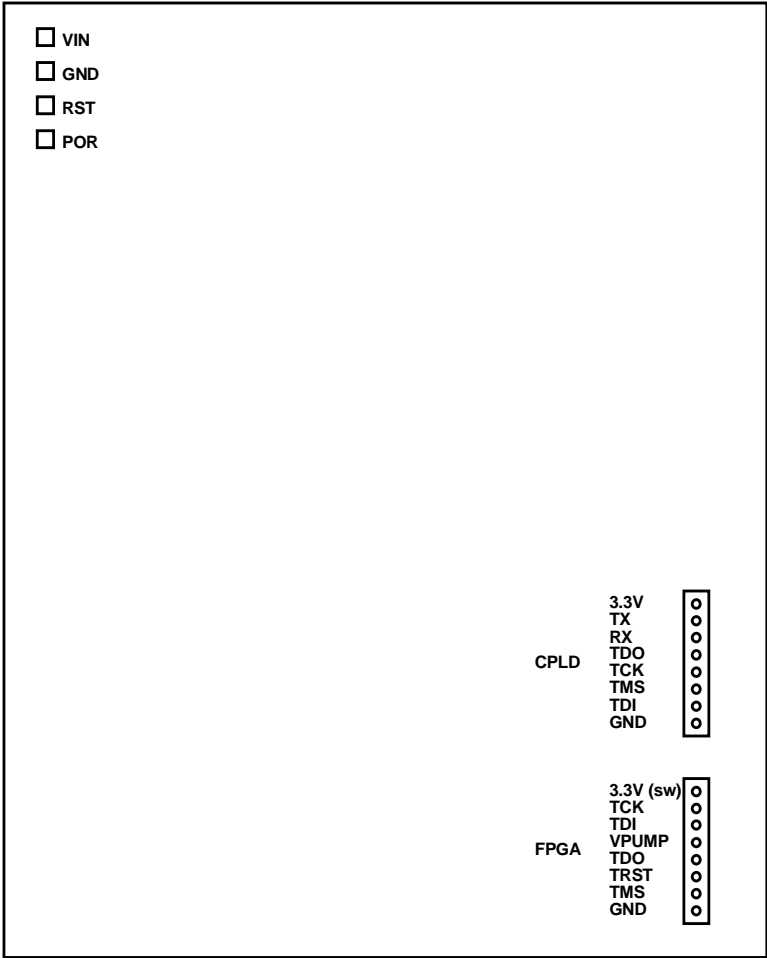


Updating Hardware

INTRODUCTION

The 41CL board uses programmable logic. This means that with the right equipment the hardware can be updated to correct errors. The same facilities that allow hardware programming can also be used to update the Flash memory on the board. This section will describe the connections necessary to perform hardware programming. The figure below shows the top side of the 41CL board.



All programming operations require that the board be powered. Using the normal HP41 connector on the bottom of the board is not an appropriate way to power the board for programming. Instead, there are three solder pads in the corner opposite the programming connectors that need to have wires soldered to them.

Solder short (20-30cm should be sufficient) wires to the solder pads labelled VIN, GND and POR. The RST solder pad is not required for programming.

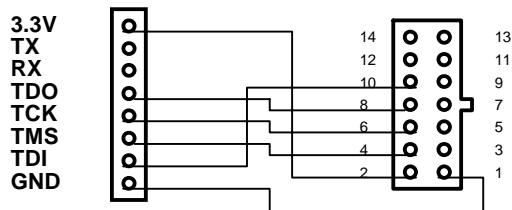
Battery power is not appropriate from programming. Instead use a benchtop power supply. The 41CL board requires 5V (4.0v minimum / 6.0V maximum) for programming.

- Make sure the power supply is OFF before connecting it to the 41CL board.
- Connect the GND wire to the ground of a benchtop power supply.
- Connect the VIN wire to the positive output from the power supply.
- Connect the POR wire to the ground of the power supply to program the FPGA or the Flash. Leave this wire unconnected to program the CPLD. Grounding the POR signal turns on the switched power supplies.

Do not turn on the power supply until the programming cable is connected. Be aware that some variable power supplies overshoot quite a bit on start-up. If you are using a variable supply it is probably better to manually ramp up the supply voltage from zero to the final value rather than turning on the supply with the full supply voltage selected.

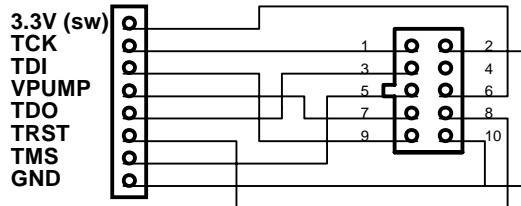
CPLD Programming

The CPLD is programmed using the connector labelled CP on the board. This is the same connector used for the serial port signals. The CPLD is programmed using a Xilinx programming cable. The figure below shows the wiring required between the CPLD connector on the board and the standard Xilinx programming cable.



FPGA Programming

The FPGA is programmed using the connector labelled FP on the board, using an Actel programming cable. The figure below shows the wiring required between the FPGA connector on the board and the standard Actel programming cable.



Flash Programming

The Flash memory is programmed using the connector labelled FP on the board. The exact connection will depend on the JTAG programming hardware that you use. The important thing to remember is that the TRST signal must be grounded to enable the JTAG controller, and the VPUMP signal must be left floating.

