Systemyde International Corporation
2129 Wedgewood Way
Livermore, CA 94550-6664

e-mail: monted@systemyde.com

Time Module Clone problem report

A 41CL user (Kari Pasanen from Finland) has reported a pair of problems with the Time Module Clone.

The first problem is specific to the 41CL and manifests itself when using the CLK24 or CLKTD modes and displaying the clock.

When the 41CL is in a Turbo mode (5x, 10x, 20x or 50x) the CLOCK function does not always display the time in the correct mode. The problem occurs at different rates depending on the Turbo mode as shown below:

5x Turbo is wrong ~40% of the time
10x Turbo is wrong ~50% of the time
20x Turbo is wrong ~50% of the time
50x Turbo is wrong ~70% of the time

The problem occurs because the Time Clone switches over from an internal clock to the 41C bus clock whenever the 41C enters the Run mode from the Light Sleep mode. This internal clock is necessary to keep time while the 41C is not running, incrementing the time every 10mS. Thus, it may take up to 10mS before the Time Clone logic is ready to be accessed by the 41 CPU using the 41C bus clock. 10mS is equivalent to sixty-four instruction times.

In a normal 41C there are sufficient instructions executed before the timer is accessed to meet this time constraint. But the same is not necessarily true for a 41CL in Turbo mode. To fix this problem, the first sixty-four instructions fetched by the 41C when entering Run mode must be executed at normal speed. This requires tagging those instructions as 1x in two .rom files:

NUT0-N.ROM - page 0 of the 41C Operating System
TIMER-3A.ROM - the Time Module code in the 41CL

These updates will be available in the next release of a Flash image for the 41CL. Both of these images are in the OS sector, which requires special handling to do the update. Refer to the update documentation for the specifics.

The second problem has to do with the RCLAF and CORRECT functions.

Because of a typo in the Verilog source code for the Time Clone, reads of the Accuracy Factor register are corrupted. Writes to the AF register are fine, and the accuracy factor circuitry works properly to compensate for crystail oscillator accuracy and drift.

On power-up the AF register is set to +0.0 which corresponds to no correction. This value will read correctly by both the RCLAF and CORRECT functions. However, any other value will be read incorrectly.

The RCLAF function is only useful for reading the current accuracy factor when changing the batteries or when doing a manual calculation for an accuracy factor adjustment. The only work-around is to record the accuracy factor outside the calculator.

The CORRECT function automatically calculates the required accuracy factor and writes it to the AF register, along with setting the time. The CORRECT function reads the AF register to determine exactly how much time has elapsed since the last setting of the time to calculate the new accuracy factor. Since any value other than +0.0 will read incorrectly, the CORRECT function can only be used one time unless the accuracy factor has been cleared to +0.0 first.

The FPGA in the Time Clone is one-time programmable, which means that this error cannot be corrected in the field. All Time Clone modules going forward will have this error corrected.

