Counter/Timer

Features

16-bit counter

Clocked by main clock, internal prescaler, or one of two external prescalers

Four outputs, with programmable set and reset count

Interrupt request on count roll-over

DMA request and dedicated DMA bus interface

Standard byte-wide interface

Description

Timer C is a sixteen-bit up-counter clocked by the main clock divided by two or sixteen, or the output of one of two external prescalers. The counter counts from zero to the limit programmed into the Timer C Divider registers and then restarts at zero. There are four Timer C outputs. Each output is controlled by a 16-set value and a 16-bit reset value. Each output is set to one when the count matches the value in the corresponding set register and is cleared when the count matches the value programmed in the corresponding reset register. This allows the creation of quadrature signals or three-phase signals with a variable frequency for motor control applications. The values in all of the Timer C registers are transferred to holding registers for use during the count cycle when the counter is reloaded with zeros, allowing the control registers to be reloaded at any time during the count cycle.

DMA channels are usually designed to work with fixed I/O addresses. To allow DMA control of Timer C, a separate Timer C Block Access Register (TCBAR) and Timer C Block Pointer Register (TCBPR) are available. The pointer register contains the address of the Timer C register to be accessed via the access register. Each read or write of the access register automatically increments the pointer register. This allows the DMA to write to a fixed internal I/O location but still program all of the relevant Timer registers.

Interface

```
module tmrc_top (dreq_tmrc, dreq2_tmrc, tcblk_rbus, tcout_reg, tmrc_int, tmrc_rbus, clkp,
                 peri_addr, pwrite_bus, resetb, tcblk_rd, tcblk_wr, tmra1_out, tmra11_out,
                 tmrc_rd, tmrc_test, tmrc_wr);

  input         clkp;          /* main peripheral clock                                  */
  input         resetb;        /* internal reset                                         */
  input         tcblk_rd;      /* timer c block access peripheral read strobe            */
  input         tcblk_wr;      /* timer c block access peripheral write strobe           */
  input         tmra1_out;     /* timer a1 output (clock enable)                         */
  input         tmra11_out;    /* timer a11 output (clock enable)                        */
  input         tmrc_rd;       /* timer c peripheral read strobe                         */
  input         tmrc_test;     /* timer c test mode                                      */
  input         tmrc_wr;       /* timer c peripheral write strobe                        */
  input   [4:0] peri_addr;     /* internal peripheral address bus                        */
  input   [7:0] pwrite_bus;    /* internal peripheral write bus                          */
  output        dreq_tmrc;     /* timer c dma request                                    */
  output        dreq2_tmrc;    /* timer c dma request 2                                  */
  output  [3:0] tcout_reg;     /* timer c output bus                                     */
  output  [3:1] tmrc_int;      /* timer c interrupt request                              */
  output  [7:0] tcblk_rbus;    /* timer c block read data bus                            */
  output  [7:0] tmrc_rbus;     /* timer c peripheral read bus                            */
```