

41C Flexible Hardware Module

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Agenda

- **A Little History**
- **The Hardware**
- **Limitations**
- **Currently Implemented Modules**
- **Other FHM possibilities**
- **A Potential Upgrade**
- **Questions?**

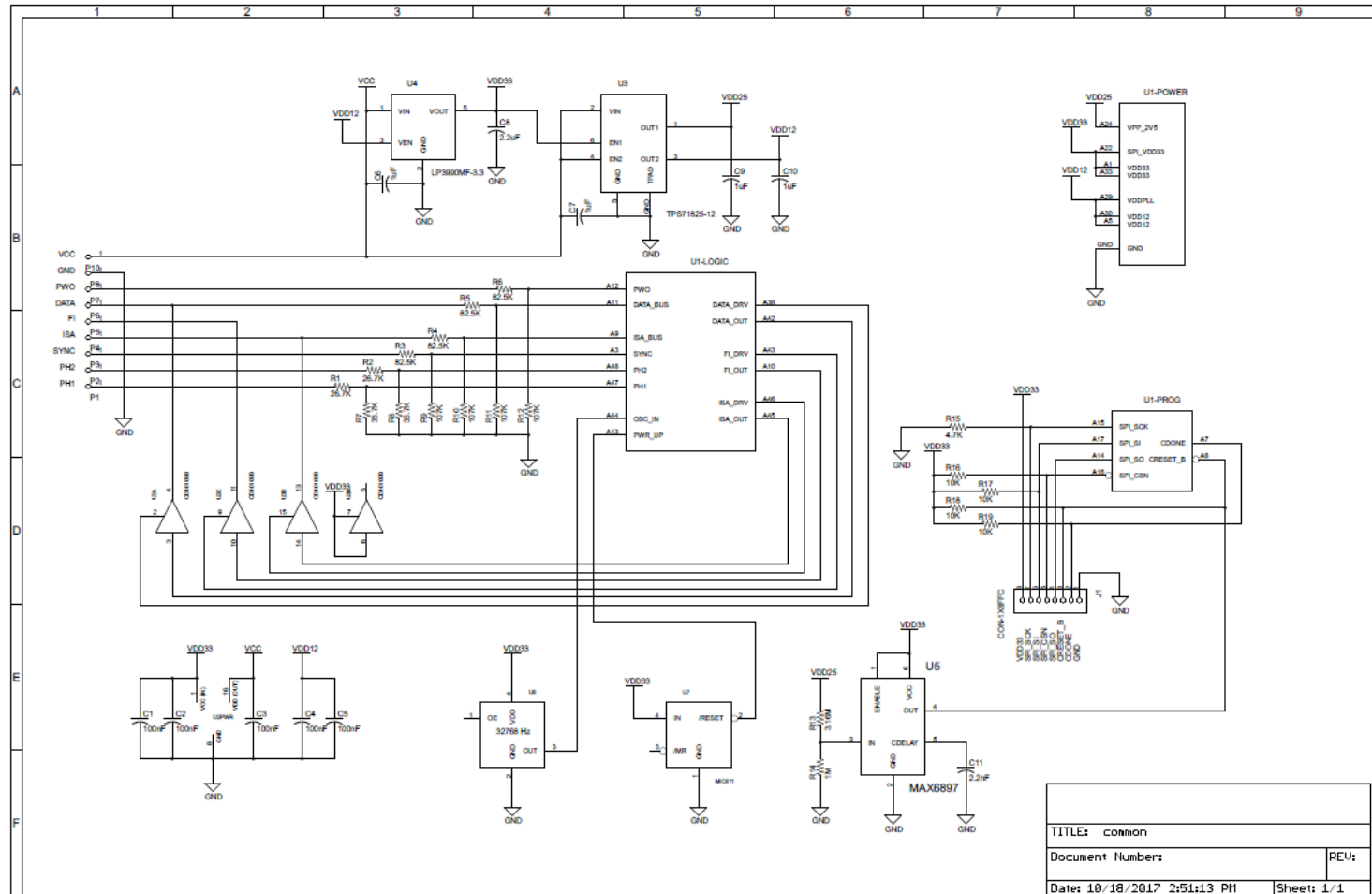
A Little History

- **2010: first version of the 41CL**
- **2011: first version of the Time clone**
(direct implementation of specification)
- **2012: second version of the Time clone**
(implemented in three Xilinx CPLD devices)
- **2015: third version of the Time clone**
(implemented in a Lattice FPGA)
- **2017: fourth version of the Time clone**
(different Lattice FPGA, PCB designed)
- **2018: converted design to Flexible Hardware Module**

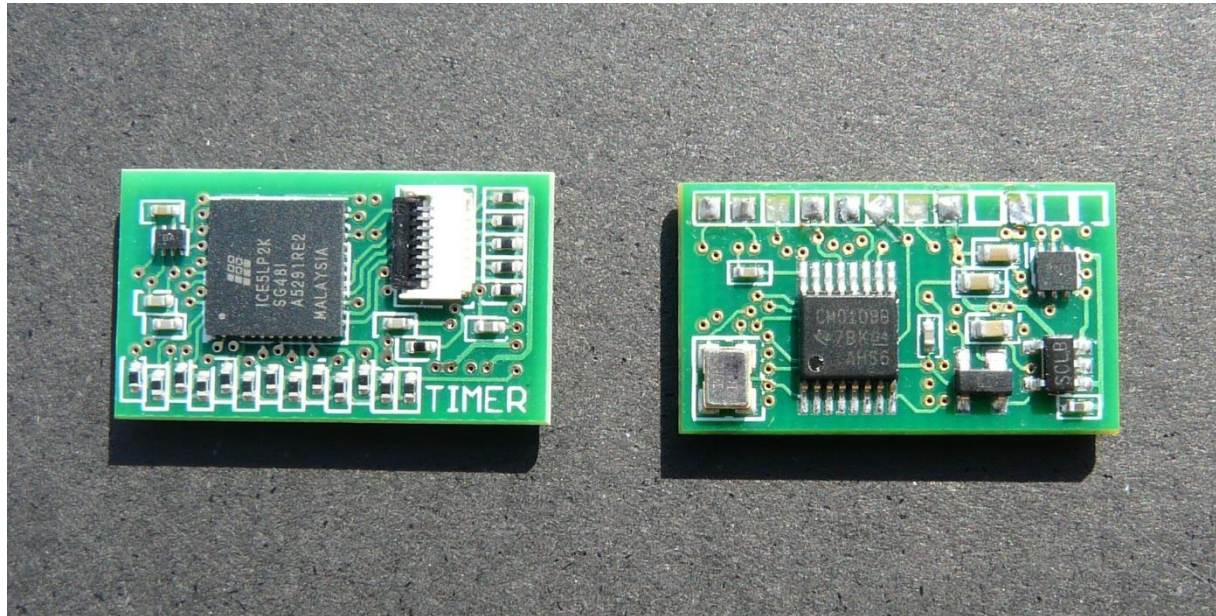
The Hardware

- Lattice iCE40Ultra FPGA
 - 2048 LUTs + 2048 FFs in a 48-QFN package
 - Twenty 4096-bit block RAMs
 - 48MHZ, 10KHz oscillators, PLL, 4x DSP, 2x SPI, 2x I2C
- 1.2V, 2.5V, 3.3V sequenced power supplies for FPGA
- 3.3V -> 6V bus drivers (ISA, DATA, FI)
- Resistor-based 6V -> 3.3V translators
- 32768Hz oscillator
- POR chip
- 8-pin FFC programming connector (4 I/O available)

FHM Schematic



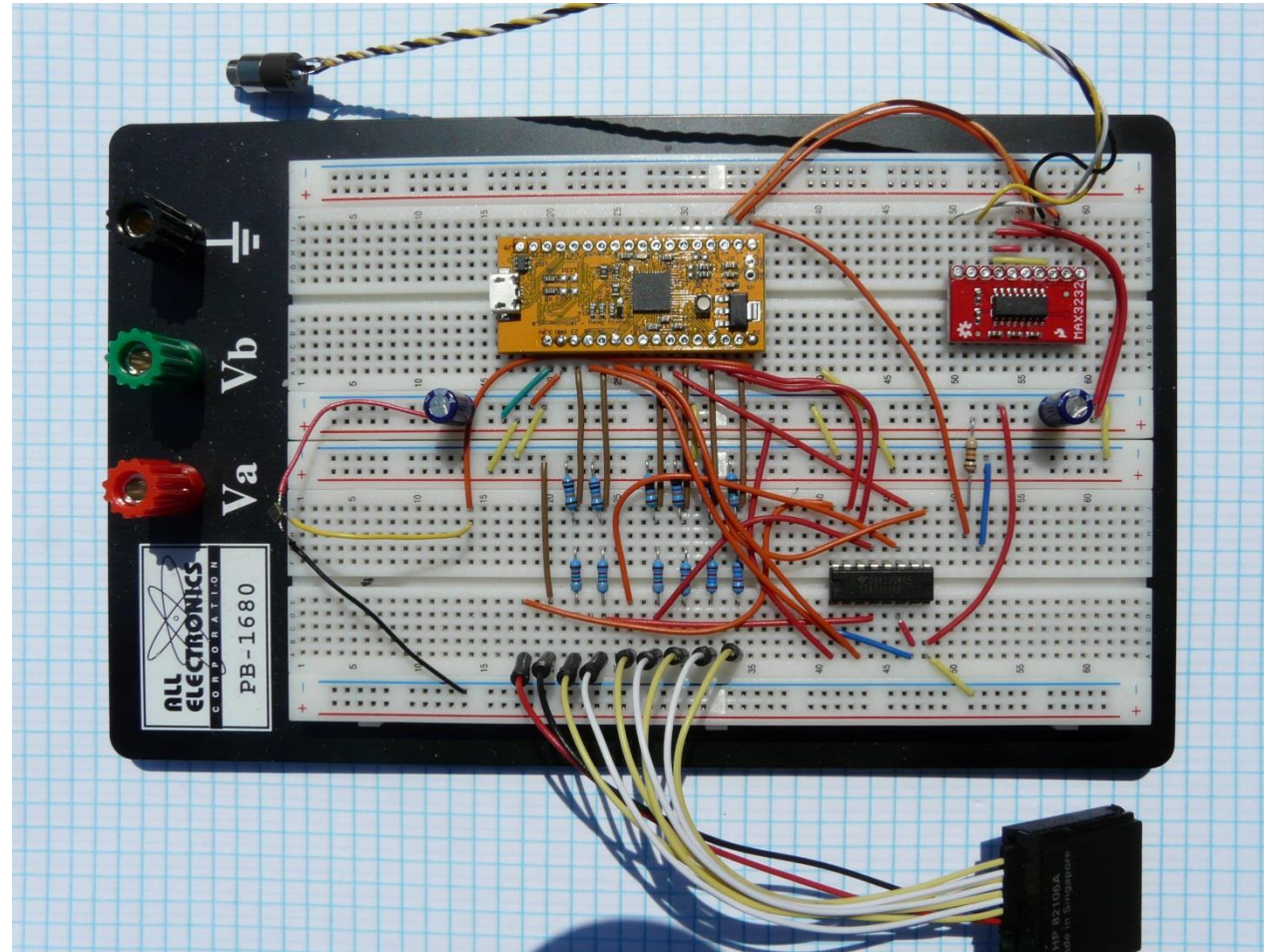
23mm x 13.2mm



Limitations

- **One-Time-Programmable FPGA**
 - Internal NVCM for programming**
 - Means that all designs must be breadboarded**
- **No Port decode hardware**
 - Fixed page decode (can be made programmable)**
- **230uA typical current drain**
- **Only four I/O available**
 - Default is three inputs, one output**
 - Inputs have resistors on the board (can be removed)**
- **Resistive level shifters optimized for 1x bus speed**

UPduino Breadboard



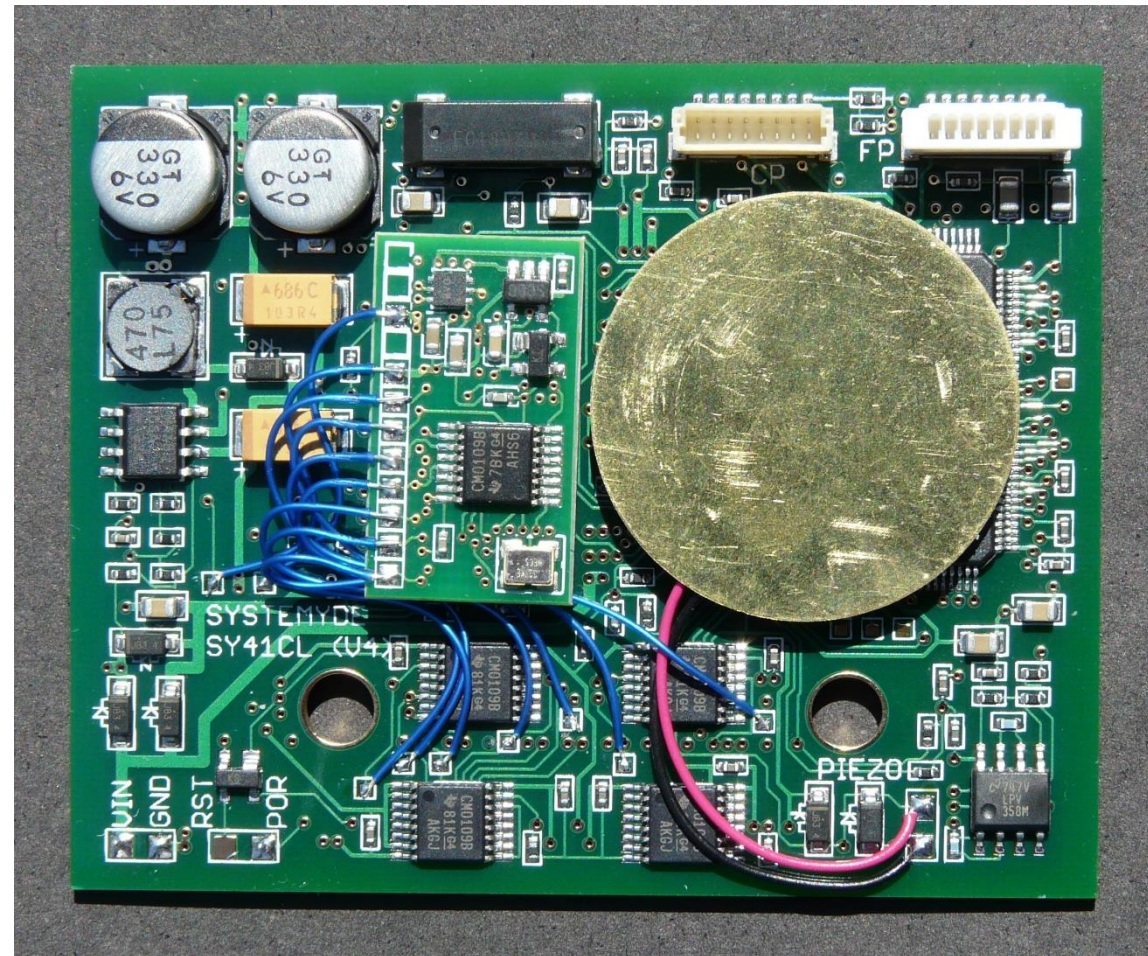
Time Module

- 834 out of 2048 LUTs
- 627 out of 2048 FFs
- 10 block RAMs for ROM

Fully functional (as far as I know)

Being shipped mounted on 41CL boards

41CL + Time Module



Time Module

The screenshot shows the Lattice iCEcube2 Floor Planner interface. The main window displays a floor plan for a project named 'timefhm'. The floor plan is a grid of logic blocks, with various colors indicating different logic instances. A vertical red bar is visible in the center of the grid. The interface includes a menu bar (File, Edit, View, Tool, Window, Help), a toolbar, and a status bar at the bottom showing 'Ln1 Col1'.

The Project Name is 'timefhm'. The Output window shows the following Logic Instance table:

Logic Instance	Instance Type	Loc
ph2_pad_gb	SB_GB	19, 1
C5600	SB_GB	12, 1
osc_in_pad	SB_GB_IO	6, 1
PH2M	SB_GB	19, 1
pwr_upb_I_0	SB_GB	6, 1
pwob_I_0	SB_GB	12, 1
PH1	SB_GB	6, 2

The Project tree on the left shows the following structure:

- Project
 - New Project
 - Open Project
 - Close Project
 - Synthesis Tool
 - Add Synthesis Files
 - Design Files
 - time_top.v
 - tim_core.v
 - imem_fpga.v
 - Constraint Files
 - Run Lattice LSE Synthesis
 - Reports
 - P&R Flow
 - Select Implementation(timefhm...)
 - timefhm.edf
 - timefhm.scf
 - Add P&R Files
 - IP Design Files
 - Constraint Files
 - generic_fhm.pcf
 - Run P&R
 - Import P&R Input Files
 - Run Placer
 - Run Router
 - Generate Bitmap
 - Output Files
 - Reports
 - time_top_pin_table.CSV
 - time_top_timing.rpt
 - placer.log
 - Bitmap
 - Simulation Netlist
 - Device/Operating Condition
 - Device Info
 - DeviceFamily: iCESLP (i...
 - Device: 2K
 - Device Package: SG48
 - Power Grade
 - Operating Condition
 - Core Voltage(V): 1.14
 - Temperature(C): 85

Time Module + 2x X-MEM

- 1058 out of 2048 LUTs
- 720 out of 2048 FFs
- 10 block RAMs for ROM
- 8 block RAMs for X-MEM

Fully functional (as far as I know) breadboard version

Time Module + 2x X-MEM

The screenshot displays the Lattice iCEcube2 Floor Planner interface. The main window shows a project named 'tmxm_fm' with a detailed logic instance table and a floor plan grid.

Logic Instance	Instance Type	Loc
ph2_pad_gb	SB_GB	19, 1
pwob_I0	SB_GB	12, 1
C5600	SB_GB	12, 1
osc_in_pad	SB_GB_IO	6, 0
PH2M	SB_GB	19, 1
pw_upb_I0	SB_GB	6, 0
PH1	SB_GB	6, 2

The floor plan grid shows a complex arrangement of logic instances, with a central vertical strip of red and green blocks. The grid is labeled with 'Ln1' and 'Col1' at the bottom right.

Project Name: tmxm_fm

Global

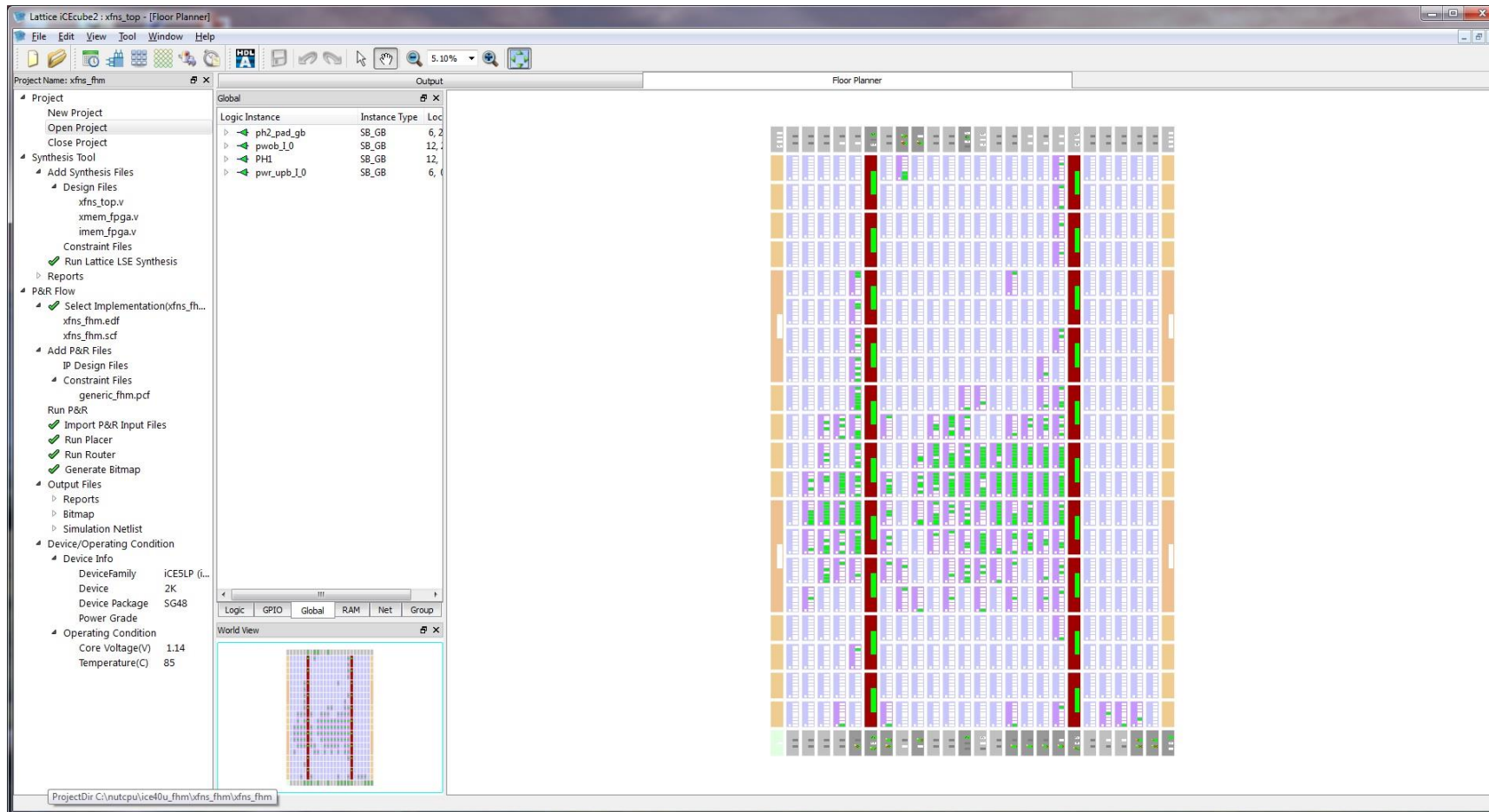
- Project
 - New Project
 - Open Project
 - Close Project
- Synthesis Tool
 - Add Synthesis Files
 - Design Files
 - tmxm_top.v
 - tim_core.v
 - xmem_fpga.v
 - imem_fpga.v
 - Constraint Files
 - Run Lattice LSE Synthesis
 - Reports
 - P&R Flow
 - Select Implementation(tm xm_f...
 - tmxm_fm.edf
 - tmxm_fm.scf
 - Add P&R Files
 - IP Design Files
 - Constraint Files
 - generic_fm.pcf
 - Run P&R
 - Import P&R Input Files
 - Run Placer
 - Run Router
 - Generate Bitmap
 - Output Files
 - Reports
 - tmxm_top_pin_table.CSV
 - tmxm_top_timing.rpt
 - placer.log
 - Bitmap
 - Simulation Netlist
 - Device/Operating Condition
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 - DeviceFamily iCESLP (i...
 - Device 2K
 - Device Package SG48
 - Power Grade
 - Operating Condition
 - Core Voltage(V) 1.14
 - Temperature(C) 85

X-FNS + 2x X-MEM

- **375 out of 2048 LUTs**
- **189 out of 2048 FFs**
- **10 block RAMs for ROM**
- **10 block RAMs for X-MEM**

Fully functional (as far as I know) breadboard version

X-FNS + 2x X-MEM



2x X-MEM

- 237 out of 2048 LUTs
- 103 out of 2048 FFs
- 8 block RAMs for X-MEM

Fully functional (as far as I know) breadboard version

2x X-MEM

The screenshot displays the Lattice iCEcube2 Floor Planner interface. The main window shows a detailed floor plan of a 2x X-MEM design, with various logic blocks and interconnects arranged in a grid. The design is color-coded, with red and green blocks indicating different logic elements. The interface includes a menu bar (File, Edit, View, Tool, Window, Help), a toolbar, and a project tree on the left. The project name is 'xmem_fm'. The output window shows the 'Global' tab with a table of logic instances.

Logic Instance	Instance Type	Loc
ph2_pad_gb	SB_GB	6, 2
PH1	SB_GB	12, 1
pwu_upb_I_0	SB_GB	6, 1
pwob_I_0	SB_GB	12, 1

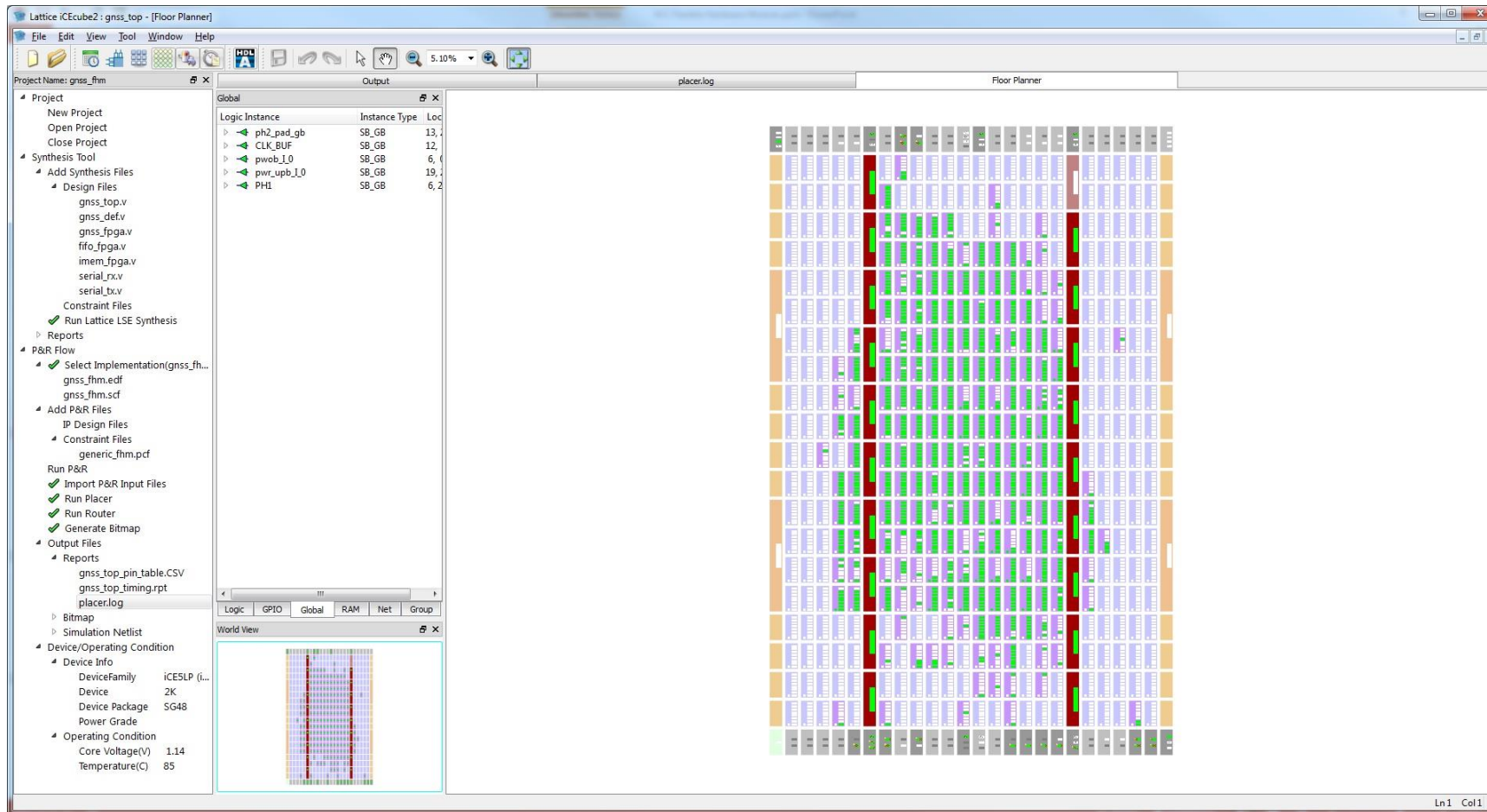
At the bottom of the project tree, the device information is displayed:

- Device Family: iCESLP (i...
- Device: 2K
- Device Package: SG48
- Power Grade:
- Operating Condition
 - Core Voltage(V): 1.14
 - Temperature(C): 85

GNSS Module

- **1259 out of 2048 LUTs**
- **763 out of 2048 FFs**
- **10 block RAMs for ROM (but it's also writable)**
- **6 block RAMs for ping-pong buffer (3 and 3)**
- **1 block RAM for 41C peripheral registers**
- **1 block RAM for receiver FIFO**
- **1 block RAM for transmitter FIFO**
- **3-wire connection FHM to GNSS receiver (rx, tx, enable)**

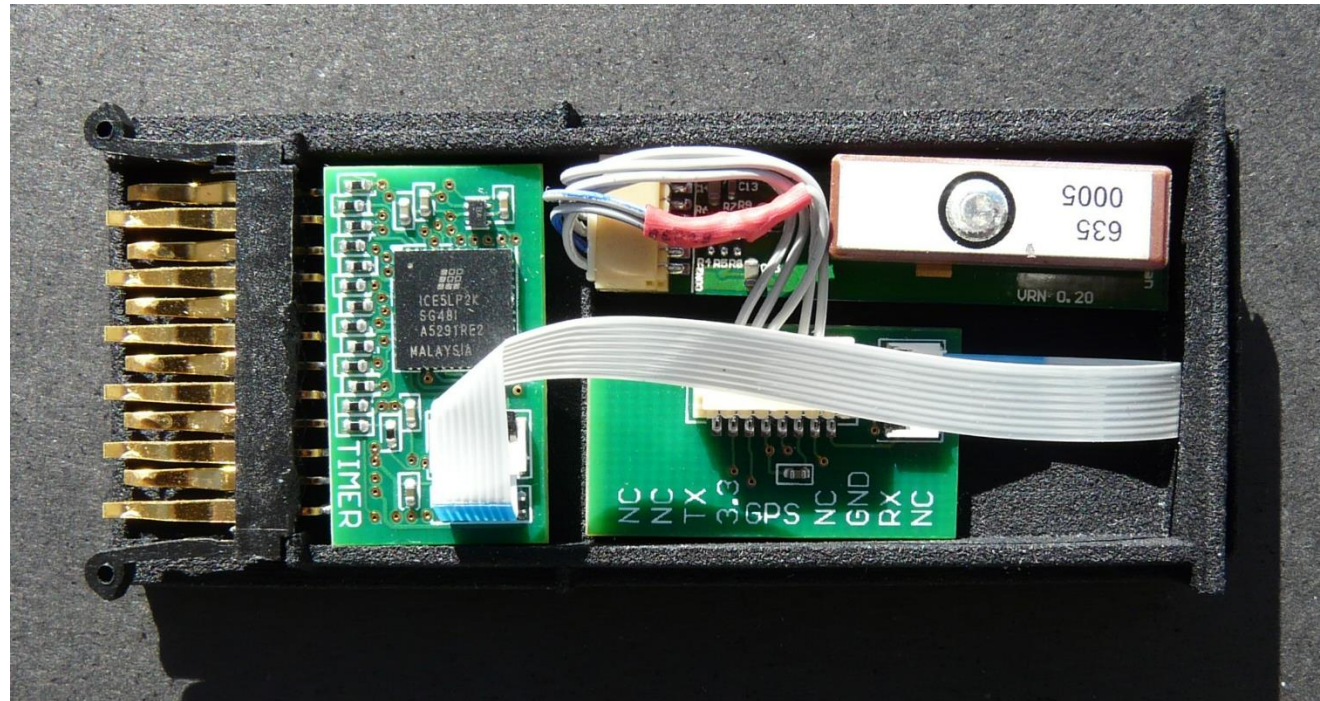
GNSS Module



GNSS Module Hardware

- Double-length module housing
- U-blox 7 GNSS receiver (8mm x 35mm x 6.5mm)
- 38.4K bit/s UART for communication
- Does as much processing as possible in hardware
 - Ping-pong buffer for NMEA messages
 - Tracks and sorts NMEA messages
 - Tracks fix status (1-d, 2-d, 3-d)
 - 41C peripheral registers for converted values
- Software in ROM provides full feature set

Inside the Module Housing



GNSS Module Software

- **Receiver Control functions (on, off, sleep, etc.)**
- **Individual GNSS Data functions (lat, lon, alt, vel, dir, etc.)**
- **Waypoint functions**
 - Lock ping-pong buffer and read fix data**
 - Write selected fix information to 41C registers**
 - Optional alpha header to identify fix information**
- **Waypoint Housekeeping functions (register pointers)**
- **Miscellaneous functions (display formats, conversions)**
- **ROM Option functions (disable, relocate, write)**
- **Possible upgrade is clock display like Time Module**

GNSS Function List

ROMID	UPDATE	CT	LLACTD	RCLWBR
GNOFF	SATS	CTX	LLACTDX	STOWBR
GNON	SATIV	CTD	LLC	RCLWPR
GNON?	GEOID	CTDX	LLCX	STOWPR
GNTRK?	HDOP	LL	LLCT	RCLRNG
DATUM	VDOP	LLX	LLCTX	WPR+X
LAT	AC	LLA	LLCTD	DMT
LON	ACX	LLAX	LLCTDX	GMODE
ALTI	ACT	LLAC	LLT	GMODE?
HEADING	ACTX	LLACX	LLTX	DISROM
SPEED	ACTD	LLACT	LLTD	ENROM
UTIME	ACTDX	LLACTX	LLTDX	RELROM
				WRROM

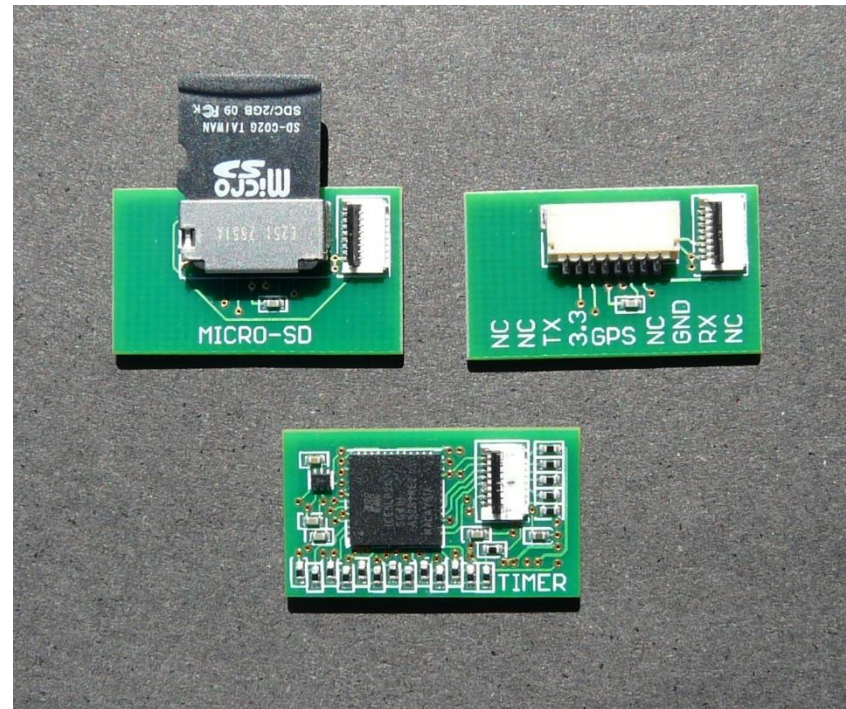
GMODE Identifiers

Functions affected	Default	Options			
Waypoint Functions	TAG	RAW			
Individual GNSS Functions	ALP	NOA			
LAT, LON	DEG	DMS	DMT		
ALTI	M	FT			
SPEED	KT	MPH	KM/H	M/S	F/S
Power Control	AUTO	GOFF	GON		
Communication Speed	384	192	96	48	
Interrupt	NOW	WAK			

Other FHM Possibilities

- SD card controller?
- Multi-protocol serial (UART, SPI, I2C) interface?
- Printer controller?
- IR printer controller?
- General-purpose IR?
- Remote display controller?
- Machine Language Development Lab?
- Barcode wand controller?
- HP-IL controller?
- What else?

FHM and Adapter Boards



Potential Upgrade

- Lattice iCE40UltraPlus

5280 LUTs + 5280 FFs in same 48-QFN package

Thirty 4096-bit block RAMs

48MHZ, 10KHz oscillators, PLL, **8x** DSP, 2x SPI, 2x I2C

Four 16k x 16 SPRAM blocks

GNSS in UltraPlus

The screenshot displays the Lattice iECube2 - [Floor Planner] software interface. The window title is "Lattice iECube2 - [Floor Planner]". The menu bar includes File, Edit, View, Tool, Window, and Help. The toolbar shows various icons for file operations and design tools. The main workspace is divided into several panes:

- Project Name:** gnss_bb
- Project:** A tree view showing the project structure, including Design Files (gnss_def.v, imem_fpga.v, serial_rx.v, serial_tx.v, fifo_fpga.v, gnss_fpga.v, gnss_top.v), Constraint Files, Reports, P&R Flow (gnss_bb.edf, gnss_bb.scf), Run P&R (Import P&R Input Files, Run Placer, Run Router, Generate Bitmap), Output Files (gnss_top_pin_table.CSV, gnss_top_timing.rpt, placer.log), and Simulation Netlist.
- Global:** A table listing Logic Instance, Instance Type, and Location. The table contains the following data:

Logic Instance	Instance Type	Loc
ph2_pad_gb	SB_GB	13, 13
CLK_BUF	SB_GB	12, 12
pwob_I0	SB_GB	6, 6
pwu_upb_I0	SB_GB	19, 19
PH1	SB_GB	6, 3
- Output:** gnss_top_sbt.rpt
- Floor Planner:** A large grid view showing the floor plan of the device. The grid is color-coded to represent different components and their placement. A small "World View" window is also visible in the bottom left corner of the main workspace.

The status bar at the bottom right indicates "Ln1 Col1".

Questions?