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Batch 71191 update (11/06/2017)

Several pages in Flash memory are not up-to-date on V5 boards shipped before the above date. The pages affected are:

0x0B7	EVAL_1F.ROM	(mnemonic FRML)
0x0B8	EVAL_APP.ROM	"
0x165	AP550-2.ROM	(mnemonic TGT2)
0x1A0	SMAT41.ROM	(mnemonic SM44)
0x1A1	SMAT42.ROM	"
0x1A6	HLMAT43.ROM	"
0x1B8	WARPB1.ROM	(mnemonic WARP)
0x1B9	WARPB2.ROM	"
0x1E5	SERIES.ROM	(mnemonic SERI)
0x1F2	ITGDIFF.ROM	(mnemonic FRID)
0x1FC	AP550-3L.ROM	(mnemonic TGT3)
0x1FD	AP550-3U.ROM	"

In addition, I discovered that UPDAT-3A has a bug that prevents certain functions from working across the entire address range. Addresses 0x200-0x2FF are affected, and the functions below should not be attempted on addresses within this range:

PGVAL
PGINV
PGUNV
PGCDB?
CDBLST?
FDBCHK?
FLCHK?
FLUPD
BFRCHK?

The *clupdate* software does not currently work with V5 boards, but that will change in the next few weeks. In the mean time, it is possible to update your V5 board to fix all of these issues if you don't want to wait. Starting from the MEMORY LOST condition:

XEQ "MMUCLR"	clear the MMU contents
"YFNX"	
XEQ "PLUG1L"	plug YFNX into page 8
"YUPS"	
XEQ "PLUG1U"	plug YUPS into page 9
XEQ "MMUEN"	enable the MMU

Turn machine OFF then ON so that YFNX is locked and YUPS internal variables are initialized. We'll load a patched YUPS over this one next.

"062>830"	
XEQ "PGCPY"	copy YUPS to RAM
"830AC2-0150"	change the protocol byte for V5 CDBEXP
XEQ YPOKE	
"830A47-0350"	change the protocol byte for V5 CDBIMP
XEQ YPOKE	
"830A49-004E"	change the protocol byte for V5 CDBIMP
XEQ YPOKE	these changes make the V5 board appear
"-830 9"	to be a V4 board to the *clupdate* program
XEQ PPLUG	plug patched YUPS into page 9

Plug the 41CL into the PC and start the *clupdate* program using the following command. Note that you need to download the current rom_files.zip file from the 41CL website to your PC before doing this.

java -jar clupdate-1.0.0.jar --update rom_files_171106.zip com3 4800

XEQ "CMOPEN"	open the comm channel
XEQ "CDBIMP"	import the CFLDB
"062"	
XEQ "PGINV"	mark 0x062 invalid to get UPDATE-3B
"0B7"	
XEQ "PGINV"	mark 0x0B7 invalid to get EVAL_1F
XEQ "PGINV"	mark 0x0B8 invalid to get EVAL_APP

"0DE"	
XEQ "PGINV"	mark 0x0DE invalid to get FLDB
"165"	
XEQ "PGINV"	mark 0x165 invalid to get AP550-2
"1A0"	
XEQ "PGINV"	mark 0x1A0 invalid to get SMAT41
XEQ "PGINV"	mark 0x1A1 invalid to get SMAT42
"1A6"	
XEQ "PGINV"	mark 0x1A6 invalid to get HLMAT43
"1B8"	
XEQ "PGINV"	mark 0x1B8 invalid to get WARPB1
XEQ "PGINV"	mark 0x1B9 invalid to get WARPB2
"1E5"	
XEQ "PGINV"	mark 0x1E5 invalid to get SERIES
"1F2"	
XEQ "PGINV"	mark 0x1F2 invalid to get ITGDIFF
"1FC"	
XEQ "PGINV"	mark 0x1FC invalid to get AP550-3L
XEQ "PGINV"	mark 0x1FD invalid to get AP550-3U
XEQ "CDBEXP"	export the CFLDB

The *clupdate* program should show 14 pages out-of-date.

"060>1FF"	update a range that covers the affected
XEQ "FLUPD"	pages. DO NOT USE "*" because this will include the 0x200 problem area!

Wait for the update to complete. It takes about 30 minutes.

XEQ "CDBEXP"

The *clupdate* program should show 0 pages out-of-date.

XEQ "CMCLOSE"	close the comm channel
"EMPT 9"	
XEQ "PPLUG"	unplug the patched YUPS

Enjoy your corrected V5 board! I apologize for my mistake, and want to thank Mark Fleming for finding the problem with these pages.